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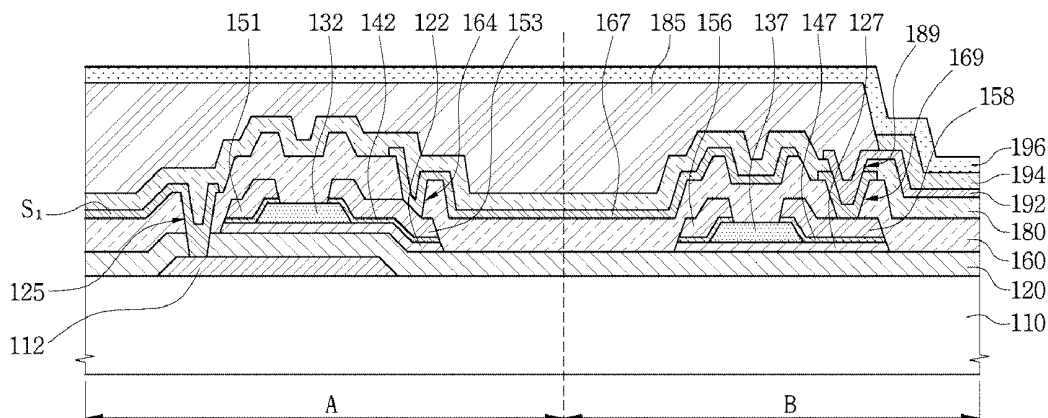


FIG. 1

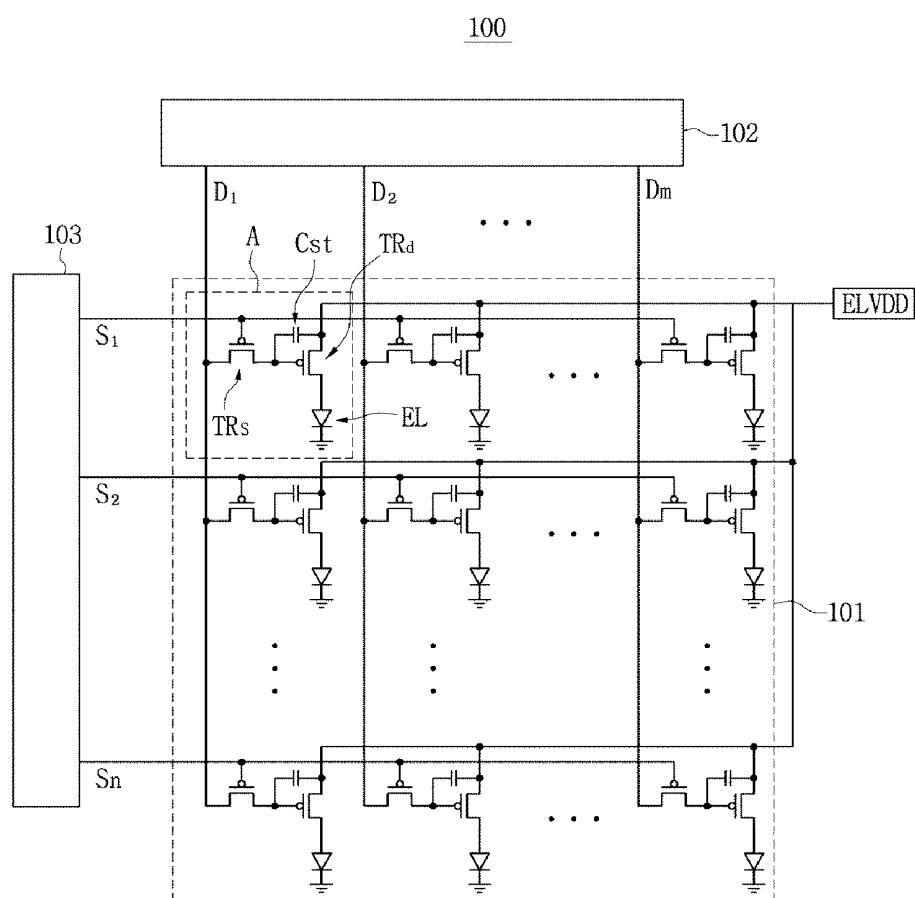


FIG. 2

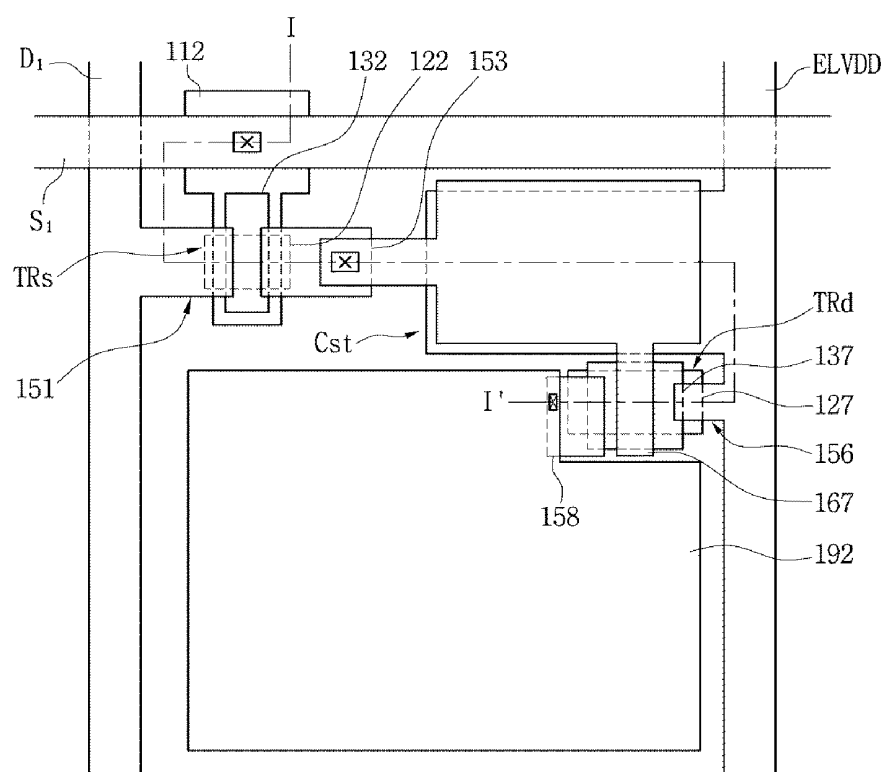


FIG. 3A

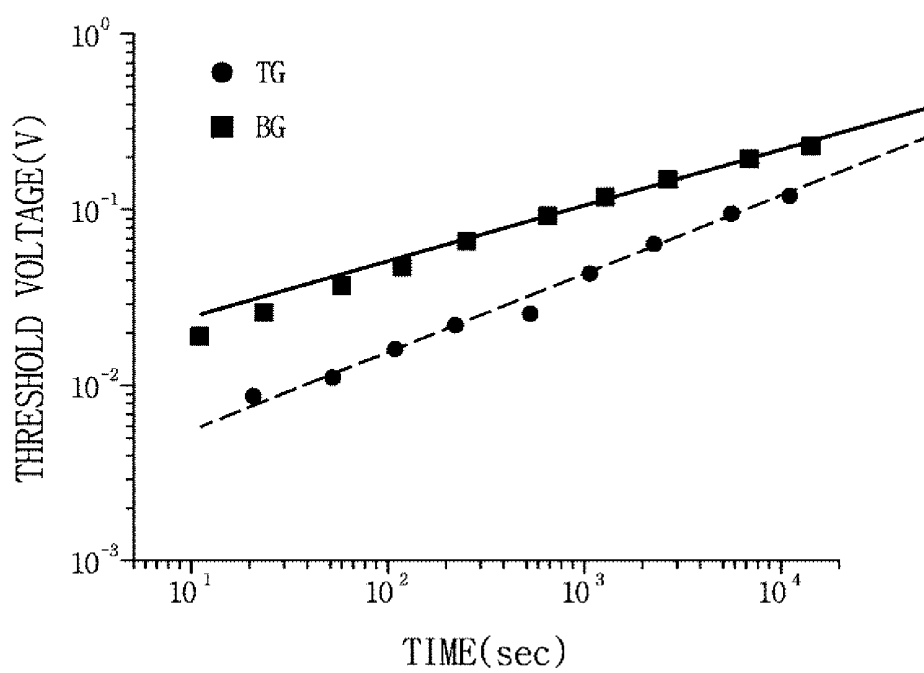


FIG. 3B

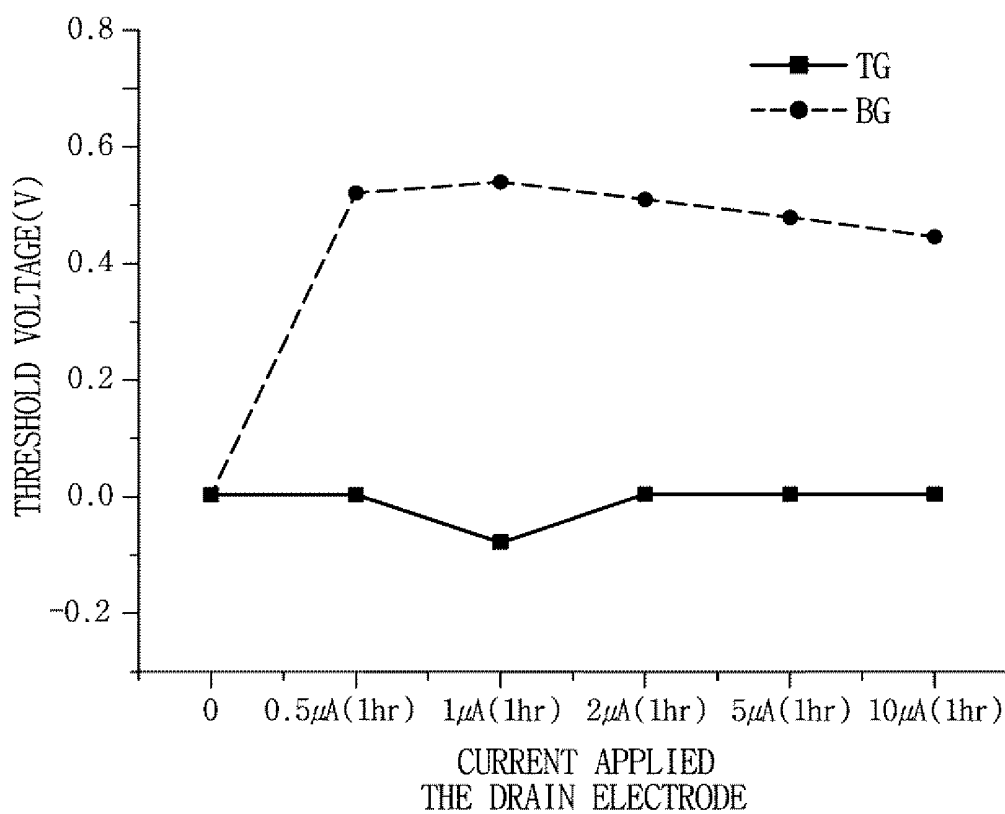


FIG. 4A

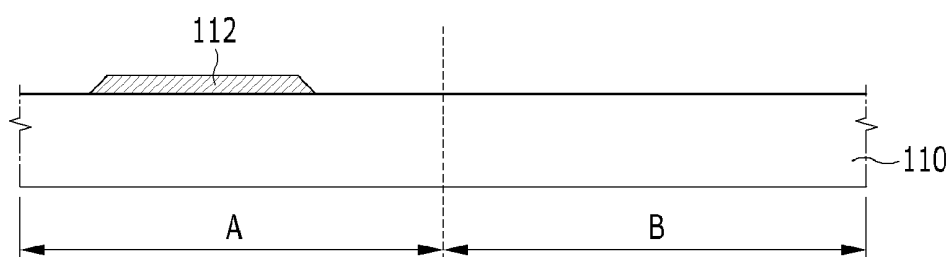


FIG. 4B

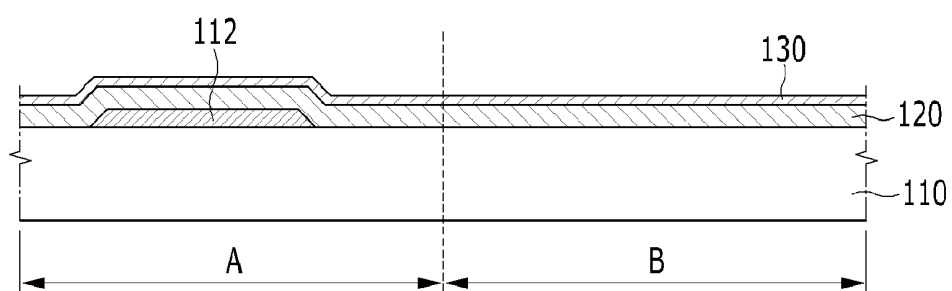


FIG. 4C

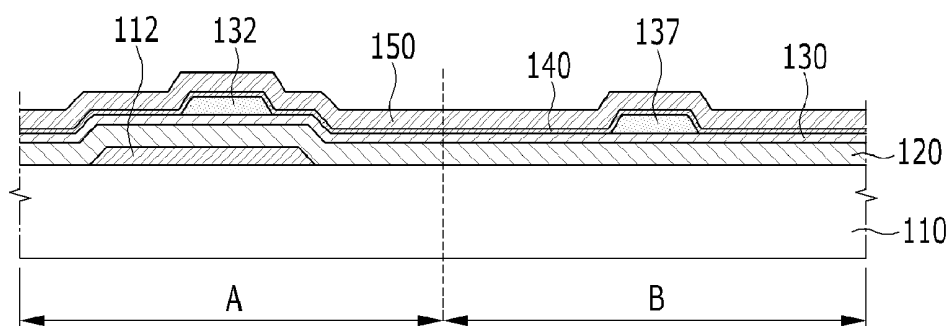


FIG. 4D

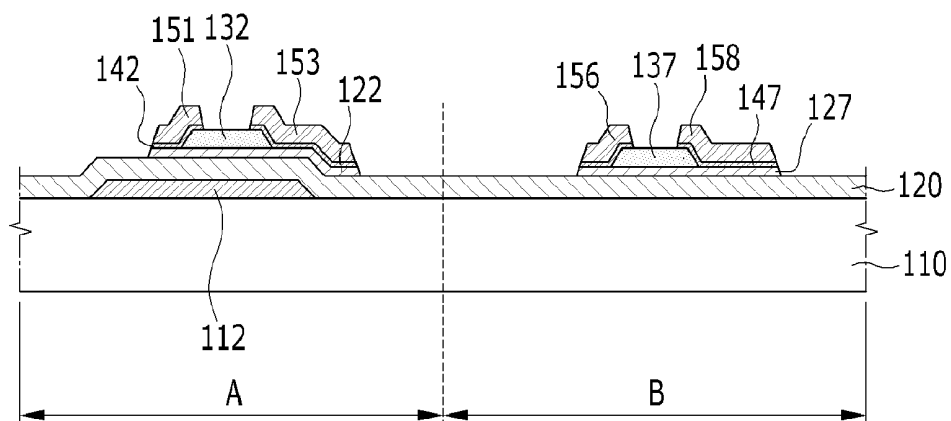


FIG. 4E

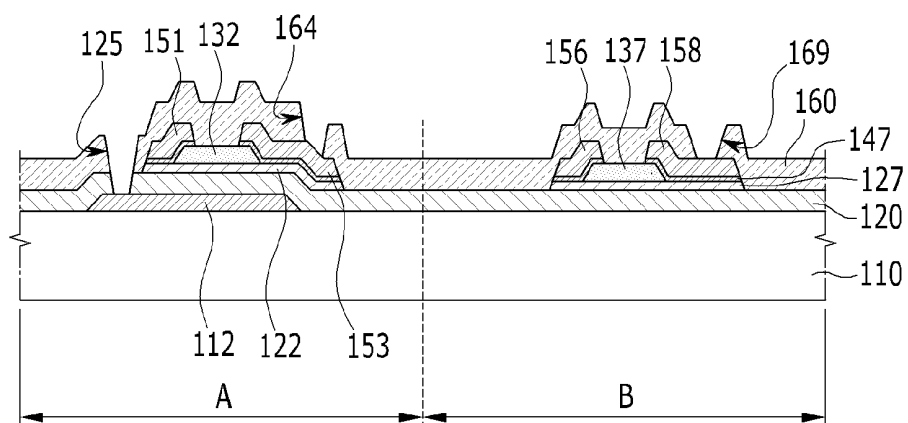


FIG. 4F

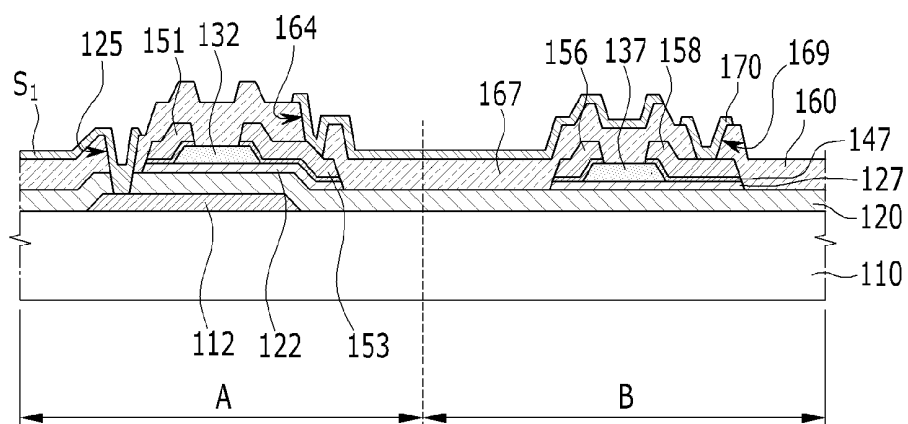
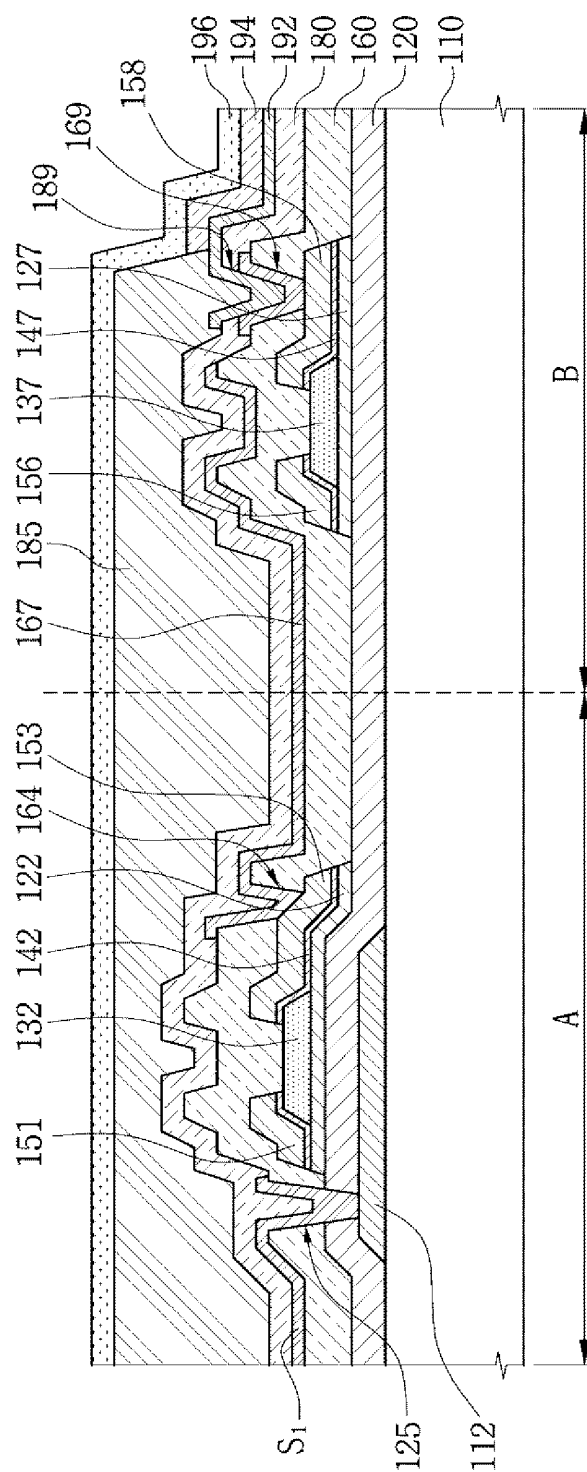


FIG. 4G



**ORGANIC LIGHT EMITTING DIODE
DISPLAY DEVICE AND METHOD OF
FABRICATING THE SAME**

**CROSS-REFERENCE TO RELATED
APPLICATIONS**

[0001] This application claims the benefit of Korean Patent Application No. 2009-108062, filed Nov. 10, 2009, the disclosure of which is hereby incorporated herein by reference in its entirety.

BACKGROUND

[0002] 1. Field

[0003] This disclosure relates to an organic light emitting diode (OLED) display device which can realize an image using an organic emitting material, and a method of fabricating the same.

[0004] 2. Description of the Related Technology

[0005] An OLED display device is a display device emitting light with a specific wavelength using energy generated from excitons generated by recombining electrons and holes, which are injected into an emitting layer from a cathode and an anode.

[0006] The OLED display devices are classified into a passive matrix type and an active matrix type. The active matrix OLED display device generally includes two thin film transistors (TFTs) to drive an organic light emitting diode (OLED) including the organic thin film. The two transistors may include a driving transistor applying a driving current to the OLED and a switching transistor transmitting a data signal to the driving transistor, thereby determining on/off of the driving transistor. Thus, compared to the passive matrix OLED display device, it has a relatively more complicated fabricating process.

[0007] The passive matrix OLED display device is typically applied in applications such as low-resolution and small-sized display devices. The active matrix OLED display device can generally exhibit stable brightness according to a uniform current provided using the switching and driving transistors disposed in each pixel of a display region, and have low power consumption, so that it can be used in high-resolution and large-sized display devices.

[0008] Generally, the thin film transistors, such as the switching or driving transistors include a semiconductor layer, a gate electrode disposed on one side of the semiconductor layer to control current flow by the semiconductor layer, and source and drain electrodes connected to opposite ends of the semiconductor layer, respectively, to transfer a certain amount of current through the semiconductor layer. The semiconductor layer may be formed of polycrystalline silicon (poly-Si) or amorphous silicon (a-Si). Since the poly-Si has a higher electron mobility than the a-Si, the poly-Si is generally more frequently used.

[0009] To form a semiconductor layer using the poly-Si, an a-Si layer is typically formed on a substrate and crystallized by one of solid phase crystallization (SPC), rapid thermal annealing (RTA), metal induced crystallization (MIC), metal induced lateral crystallization (MILC), excimer laser annealing (ELA), and sequential lateral solidification (SLS).

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0010] Embodiments of the present invention provide an OLED display device which can prevent a decrease in process

efficiency and increase emitting efficiency by forming a switching transistor and a driving transistor in structures suitable for different roles in each pixel through a relatively simple process, and a method of fabricating the same.

[0011] One aspect is an organic light emitting diode (OLED) display device, including: a plurality of scan lines, a plurality of data lines, and a plurality of pixels disposed in a region in which the scan lines cross the data lines, where each pixel of the plurality of pixels includes: a switching transistor including a first gate electrode, a first semiconductor layer disposed over the first gate electrode, a first gate insulating layer interposed between the first gate electrode and the first semiconductor layer, a first source electrode and a first drain electrode, a driving transistor including a second semiconductor layer, a second gate electrode disposed over the second semiconductor layer, a second gate insulating layer interposed between the second gate electrode and the second semiconductor layer, a second source electrode and a second drain electrode, and an organic light emitting diode electrically connected with the second source and second drain electrodes of the driving transistor, where the first and second semiconductor layers are formed of the same material, and from the same processing.

[0012] The first and second semiconductor layers may be formed of polycrystalline silicon (poly-Si).

[0013] The poly-Si for the first and second semiconductor layers may have the same crystalline structure.

[0014] Each pixel may further include a first ohmic contact layer interposed between the first semiconductor layer and the first source and first drain electrodes, and a second ohmic contact layer interposed between the second semiconductor layer and the second source and second drain electrodes.

[0015] The first and second ohmic contact layers may be formed of amorphous silicon doped with impurities.

[0016] Each pixel may further include a first etch stop layer disposed on a partial region of the first semiconductor layer, and a second etch stop layer disposed on a partial region of the second semiconductor layer.

[0017] The OLED may include a lower electrode electrically connected with the second source and second drain electrodes, an organic layer disposed over the lower electrode and including one or more emission layers, and an upper electrode disposed over the organic layer.

[0018] The second gate electrode may be disposed over the second source and second drain electrodes.

[0019] The first source and first drain electrodes may be formed of the same material and from the same processing as the second source and drain electrodes.

[0020] Another aspect is a method of fabricating an organic light emitting diode (OLED) display device, including: providing a substrate having first and second regions, forming a first gate electrode over the first region of the substrate, forming a first gate insulating layer over the first gate electrode, forming a polycrystalline silicon (poly-Si) layer over the first gate insulating layer, forming a conductive material layer over the poly-Si layer, etching the poly-Si layer and the conductive material layer, and forming a first semiconductor layer, a first source electrode and a first drain electrode in the first region, and a second semiconductor layer, a second source electrode and a second drain electrode in the second region, where the first and second semiconductor layers are formed of the same material from the same processing, forming a second gate insulating layer over the first and second source and drain electrodes, forming a second gate electrode

over the second region of the second gate insulating layer, forming a protective layer on the second gate electrode, etching the protective layer and the second gate insulating layer, and forming a via hole exposing one of the second source and drain electrodes, and forming an OLED including a lower electrode electrically connected with the second source and drain electrodes through the via hole on the protective layer.

[0021] The method may further include crystallizing the a-Si layer into the poly-Si layer.

[0022] The method may further include: forming an amorphous silicon layer over the poly-Si layer, forming a conductive material layer over the a-Si layer, and etching the a-Si layer doped with impurities through an etching process for the poly-Si layer and the conductive material layer, and forming a first ohmic contact layer between the first semiconductor layer and the first source and first drain electrodes, and a second ohmic contact layer between the second semiconductor layer and the second source and second drain electrodes.

[0023] The method may further include forming a first etch stop layer over a first region of the poly-Si layer and a second etch stop layer over a second region of the poly-Si layer.

[0024] The method may further include forming the first and second etch stop layers along partial regions of the first and second semiconductor layers.

[0025] The method may further include: etching the second gate insulating layer and forming a first contact hole exposing one of the first source and drain electrodes, and electrically connecting the second gate electrode with the first source and first drain electrodes through a second contact hole.

[0026] The method may further include: etching the second gate insulating layer and forming a second contact hole exposing one of the second source and second drain electrodes, forming an interconnection electrically connected with the second source and second drain electrodes through the second contact hole along with the second gate electrode, and electrically connecting the lower electrode with the interconnection by exposing the interconnection through the via hole.

[0027] The method may further include forming the first and second gate electrodes using the same material and the same process.

[0028] The OLED may be formed by forming a pixel defining layer partially exposing the lower electrode over the protective layer, forming an organic layer including one or more emission layers over the lower electrode exposed by the pixel defining layer, and forming an upper electrode over the organic layer.

[0029] The method may further include: forming a planarization layer over the protective layer, forming a via hole by etching the protective layer and the planarization layer, and forming a lower electrode electrically connected with the second source and second drain electrodes through the via hole over the planarization layer.

[0030] Additional aspects and/or advantages of embodiments of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The above and other objects, features and advantages will be described in reference to the attached drawings in which:

[0032] FIG. 1 is a schematic diagram of an embodiment of an OLED display device;

[0033] FIG. 2 is a plan view of a single pixel of an embodiment of the OLED display device;

[0034] FIGS. 3A and 3B are graphs showing comparison of driving characteristics between an inverted staggered (BG) thin film transistor and a staggered (TG) thin film transistor; and

[0035] FIGS. 4A through 4G are cross-sectional views sequentially illustrating an embodiment of a method of fabricating an embodiment of an OLED display device.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0036] Embodiments of the present invention will now be described more fully hereinafter with reference to the accompanying drawings. Like numerals generally denote the like elements throughout the specification, and when one element is “connected with another element, these elements may be “directly connected” with each other, or “electrically connected” with each other having another element therebetween. Moreover, in the drawings, thicknesses of layers and regions may be exaggerated for clarity.

[0037] An active matrix OLED display device generally includes switching and driving transistors having the same structure in each pixel. The driving transistor is to provide a certain minimum amount of driving current to the OLED. Thus, high current drivability is typically required in driving transistors. On the other hand, the switching transistor should typically maintain a low leakage current as it has to accurately determine the on/off state of the driving transistor. However, typically the switching and driving transistors are fabricated to have the same structure to maintain or improve manufacturing efficiency. Accordingly, the switching and driving transistors in the same structure cannot adequately satisfy the different roles thereof, which may result in a decrease in emitting efficiency.

[0038] To better fulfill the different roles, the switching and driving transistors are designed differently and manufactured separately, which may result in a possible decrease in manufacturing process efficiency. According to various embodiments of the present invention, the switching transistor and driving transistor are in different configurations while minimizing decrease in manufacturing efficiency. FIG. 1 is a schematic diagram of an embodiment of an OLED display device, and FIG. 2 is a plan view of a single pixel of an embodiment of the OLED display device.

[0039] Referring to FIGS. 1 and 2, an embodiment of the OLED display device 100 includes a pixel part 101, which displays an image, a data driver 102, which applies a data signal to the pixel part 101 through a plurality of data lines D1 through Dm, and a scan driver 103, which applies a scan signal to the pixel part 101 through a plurality of scan lines S1 through Sn. The pixel part 101 includes a plurality of pixels P disposed in a region in which the scan lines cross the data lines.

[0040] Each pixel P includes (1) an OLED emitting layer (EL) expressing a color in response to the data signal, (2) a driving transistor TRd providing a driving current to the OLED EL in response to the data signal, (3) a switching transistor TRs transmitting the data signal in response to the scan signal to turn on/off the driving transistor TRd, and (4) a capacitor Cst storing a voltage corresponding to the data signal. In some embodiments, the pixel P may further include

a plurality of thin film transistors (not shown) and capacitors (not shown) to compensate a threshold voltage of the driving transistor TRd.

[0041] The switching transistor TRs includes a first gate electrode **112** electrically connected with one of the scan lines S1 through Sn, a first semiconductor layer **122** disposed on the first gate electrode **112**, and first source/drain electrodes **151** and **153** electrically connected with opposite ends of the first semiconductor layer **122**.

[0042] The driving transistor TRd includes a second semiconductor layer **127** disposed on the same layer as the first semiconductor layer **122**, a second gate electrode **167** disposed on the second semiconductor layer **127**, and second source and drain electrodes **156** and **158** electrically connected with opposite ends of the second semiconductor layer **127**. In some embodiments, the second gate electrode **167** may be electrically connected with the drain electrode **153**.

[0043] FIGS. 3A and 3B are graphs showing comparisons of driving characteristics between an inverted staggered (BG) thin film transistor in which a gate electrode is disposed under a semiconductor layer and a staggered (TG) thin film transistor in which a semiconductor layer is disposed under a gate electrode. In other words, in an inverted staggered (BG) thin film transistor, the gate electrode is disposed between the substrate and the semiconductor layer, whereas in a staggered (TG) thin film transistor, the semiconductor layer is disposed between the substrate and the gate electrode. FIG. 3A illustrates a change in threshold voltage according to time when -20 V is applied to the gate electrode, and FIG. 3B illustrates a change in threshold voltage according to a current applied to the drain electrode when 10 V is applied to the gate electrode.

[0044] Referring to FIG. 3A, when an amount of negative voltage is continuously applied to the gate electrode, a slope of the change in threshold voltage according to time is 0.4577 for the staggered (TG) thin film transistor, and 0.3212 for the inverted staggered (BG) thin film transistor. Compared to the staggered (TG) thin film transistor, the inverted staggered (BG) thin film transistor has relatively less change in threshold voltage according to time.

[0045] Referring to FIG. 3B, when an amount of positive voltage is continuously applied to the gate electrode, and a current applied to the drain electrode is increased over time, 0.08 V of a threshold voltage transfers in the staggered (TG) thin film transistor, and 0.54 V of a threshold voltage transfers in the inverted staggered (BG) thin film transistor. The staggered (TG) thin film transistor has relatively less change in threshold voltage according to the change in current applied to the drain electrode than the inverted staggered (BG) thin film transistor. In other words, the change in drain electric field is lower in the staggered (TG) thin film transistor than in the inverted staggered (BG) thin film transistor.

[0046] Accordingly, to transmit a data signal in response to the scan signal, an embodiment of the OLED display device **100** may include an inverted staggered (BG) thin film transistor as the switching transistor TRs, which ideally exhibits a low leakage current, and a staggered (TG) thin film transistor as the driving transistor TRd, which generally requires a high driving characteristic. These transistors would produce and apply various driving currents to the OLED EL in response to the data signal. Thus, the OLED display device **100** may exhibit improved emitting efficiency.

[0047] FIGS. 4A through 4G are cross-sectional views taken along line I-I' of FIG. 2, and illustrate an embodiment of a method of fabricating an embodiment of an OLED display device **100**.

[0048] As shown in FIG. 4A, an embodiment of an OLED display device **100** includes a first conductive material layer (not shown) formed on a substrate **110** having a first region A and a second region B. The substrate may be formed of glass, synthetic resin, or stainless steel. The OLED display device further includes a first gate electrode **112** disposed on the first region A of the substrate **110**, formed by etching the first conductive material layer. In some embodiments, the first conductive material layer may be a metal layer formed in a single layer of aluminum (Al) or an Al alloy such as aluminum-neodymium (Al—Nd), or a multiple layer in which an Al alloy is stacked on a chromium (Cr) or molybdenum (Mo) alloy.

[0049] As shown in FIG. 4B, a first gate insulating layer **120** is formed on the substrate **110** including the first gate electrode **112**, and a poly-Si layer **130** is formed on the first gate insulating layer **120**. In some embodiments, to form the poly-Si layer **130** on the first gate insulating layer **120**, an a-Si layer (not shown) may be deposited on the first gate insulating layer **120**, and then crystallized into the poly-Si layer **130** by a method selected from SPC, RTA, MIC, MILC, ELA, and SLS.

[0050] As shown in FIG. 4C, after the a-Si layer **140** is formed on the poly-Si layer **130**, the a-Si layer **140** is doped with P-type or N-type impurities, and a second conductive material layer **150** is formed on the a-Si layer **140**. In some embodiments, the second conductive material layer **150** may be formed of molybdenum-tungsten (MoW), aluminum (Al), or an Al alloy such as Al-neodymium (Nd).

[0051] In some embodiments, in order to prevent deterioration of the driving characteristics of the first and second semiconductor layers **122** and **127** formed by etching the poly-Si layer **130** due to damage to a surface of the poly-Si layer **130** during a subsequent etching process, a first etch stop layer **132** and a second etch stop layer **137** may be formed on the poly-Si layer **130**.

[0052] As shown in FIG. 4D, the first and second etch stop layers **132** and **137** are formed to correspond to partial regions of the first and second semiconductor layers **122** and **127** to be formed by a subsequent process. In such embodiments, electrical connections between the first semiconductor layer **122** and the first source and drain electrodes **151** and **153** and between the second semiconductor layer **127** and the second source and drain electrodes **156** and **158** may be easily formed.

[0053] Still referring to FIG. 4D, the poly-Si layer **130**, the a-Si layer **140** doped with impurities, and the second conductive material layer **150** are etched, thereby forming a first semiconductor layer **122** disposed in the first region A. First source and drain electrodes **151** and **153** are electrically connected with opposite ends of the first semiconductor layer **122**, a first ohmic contact layer **142** is interposed between the first semiconductor layer **122** and the first source and drain electrodes **151** and **153**, and a second semiconductor layer **127** is disposed in the second region B. Second source and drain electrodes **156** and **158** are electrically connected with opposite ends of the second semiconductor layer **127**, and a second ohmic contact layer **147** is interposed between the second semiconductor layer **127** and the second source and drain electrodes **156** and **158**.

[0054] In some embodiments, the first and second semiconductor layers 122 and 127 are electrically connected with the first source and drain electrodes 151 and 153 or the second source and drain electrodes 156 and 158 through the first and second ohmic contact layers 142 and 147 formed of the a-Si doped with impurities. In other embodiments, the first and second ohmic contact layers 142 and 147 may be formed of poly-Si, source and drain regions (not shown) and a channel region (not shown) may be formed by doping partial regions of the first and second semiconductor layers 122 and 127 with impurities, and the first source and drain electrodes 151 and 153 may be connected with the source and drain regions of the first semiconductor layer 122, and the second source and drain electrodes 156 and 158 may be connected with the source and drain regions of the second semiconductor layer 127.

[0055] In some embodiments, the poly-Si layer 130, the a-Si layer 140 doped with impurities and the second conductive material layer 150 may be sequentially stacked and etched, the poly-Si layer 130 may be etched before the formation of the a-Si layer 140 to form the first and second semiconductor layers 122 and 127, the a-Si layer 140 doped with impurities may be formed on the first and second semiconductor layers 122 and 127, and the a-Si layer 140 doped with impurities may be etched before the formation of the second conductive material layer 150 to form the first and second ohmic contact layers 142 and 147.

[0056] As shown in FIG. 4E, a second gate insulating layer 160 is formed on the first source and drain electrodes 151 and 153 and the second source and drain electrodes 156 and 158, and etched to form a first contact hole 164 partially exposing the first drain electrode 153 of the first source and drain electrodes 151 and 153, a second contact hole 169 partially exposing the second drain electrode 158 of the second source and drain electrodes 156 and 158, and a third contact hole 125 partially exposing the first gate electrode 112.

[0057] In some embodiments, the first drain electrode 153 is partially exposed through the first contact hole 164, and the second drain electrode 158 is partially exposed through the second contact hole 169, the first source electrode 151 may be partially exposed through the first contact hole 164, and the second source electrode 156 may be partially exposed through the second contact hole 169.

[0058] In some embodiments, the first gate electrode 112 and the scan line S1 may be independently formed. In other embodiments, the first gate electrode 112 may be simultaneously formed with the scan line S1.

[0059] As shown in FIG. 4F, a third conductive material layer (not shown) is formed on the second gate insulating layer 160, and etched to form a scan line S1, a second gate electrode 167 electrically connected with the first drain electrode 153 through the first contact hole 164, and an interconnection 170 electrically connected with the second drain electrode 158.

[0060] In some embodiments, the third conductive material layer may be a metal layer formed in a single layer of Al or an Al alloy such as Al—Nd, or a multiple layer in which an Al alloy is stacked on a Cr or Mo alloy, and may be formed of the same material as the first conductive material layer.

[0061] As shown in FIG. 4G, a protection layer 180 is formed on the scan line S1, the second gate electrode 167, and the interconnection 170, and etched to form a via hole 189 partially exposing the interconnection 170, a lower electrode 192 electrically connected with the interconnection 170

through the via hole 189, an organic layer 194 disposed on the lower electrode 192 and including one or more emission layers (not shown), and an upper electrode 196 disposed on the organic layer 194, and thus an OLED is completed.

[0062] In some embodiments, to separate adjacent pixels from each other, a pixel defining material layer (not shown) is formed of one selected from the group consisting of polyimide, benzocyclobutene series resin, phenol resin, and acrylate and etched to form a pixel defining layer 185 partially exposing the lower electrode 192, and the organic layer 194 is formed on the lower electrode 192 exposed by the pixel defining layer 185.

[0063] The protective layer 180 may be formed of silicon oxide (SiO₂), silicon nitride (SiN_x) or a combination thereof, and a planarization layer (not shown) may be further formed of an organic insulating layer of acryl or an inorganic insulating layer of silicon oxide on the protective layer 180.

[0064] In some embodiments, a lower electrode 192 of the OLED may be electrically connected with the second drain electrode 158 through the interconnection 170. The second contact hole 169 may be simultaneously formed with the via hole 189 for the lower electrode 192 to be in direct contact with the second drain electrode 158. However, because of a step difference between the thicknesses of the second gate insulating layer 192 and the protection layer 180, the lower electrode 192 may be short-circuited with the second drain electrode 158.

[0065] In some embodiments, the gate electrode of the switching transistor is formed, the semiconductor layer of the switching transistor is simultaneously formed with the semiconductor layer of the driving transistor, and the gate electrode of the driving transistor is formed on the semiconductor layer. Thus, in each pixel, the switching transistor and the driving transistor, which have different structures for fulfilling different roles, may be formed with a relatively simple process.

[0066] In embodiments of the OLED display device and methods of fabricating the same, a switching transistor maintaining a low leakage current by forming one poly-Si layer and a driving transistor having a high drivability are formed, thereby increasing emitting efficiency of the OLED display device in a relatively simple manufacturing process.

[0067] Although certain embodiments of the present invention have been described, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the embodiments without departing from the spirit or scope of the present invention defined in the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting diode (OLED) display device, comprising:

a plurality of scan lines, a plurality of data lines, and a plurality of pixels disposed in a region in which the scan lines cross the data lines,

wherein each pixel of the plurality of pixels comprises:

a switching transistor comprising a first gate electrode, a first semiconductor layer disposed over the first gate electrode, a first gate insulating layer interposed between the first gate electrode and the first semiconductor layer, a first source electrode and a first drain electrode;

a driving transistor comprising a second semiconductor layer, a second gate electrode disposed over the second semiconductor layer, a second gate insulating layer

interposed between the second gate electrode and the second semiconductor layer, a second source electrode and a second drain electrode; and
an organic light emitting diode electrically connected with the second source and second drain electrodes of the driving transistor.

2. The device according to claim 1, wherein the first and second semiconductor layers are formed of polycrystalline silicon (poly-Si).

3. The device according to claim 2, wherein the poly-Si for the first and second semiconductor layers has the same crystalline structure.

4. The device according to claim 1, wherein each pixel further comprises a first ohmic contact layer interposed between the first semiconductor layer and the first source and first drain electrodes, and a second ohmic contact layer interposed between the second semiconductor layer and the second source and second drain electrodes.

5. The device according to claim 4, wherein the first and second ohmic contact layers are formed of amorphous silicon doped with impurities.

6. The device according to claim 1, wherein each pixel further comprises a first etch stop layer disposed on a partial region of the first semiconductor layer, and a second etch stop layer disposed on a partial region of the second semiconductor layer.

7. The device according to claim 1, wherein the OLED includes a lower electrode electrically connected with the second source and second drain electrodes, an organic layer disposed over the lower electrode and including one or more emission layers, and an upper electrode disposed over the organic layer.

8. The device according to claim 1, wherein the second gate electrode is disposed over the second source and second drain electrodes.

9. The device according to claim 1, wherein the first source and first drain electrodes are formed of the same material as the second source and drain electrodes.

10. A method of fabricating an organic light emitting diode (OLED) display device, comprising:

providing a substrate having first and second regions;
forming a first gate electrode over the first region of the substrate;
forming a first gate insulating layer over the first gate electrode;
forming a polycrystalline silicon (poly-Si) layer over the first gate insulating layer;
forming a conductive material layer over the poly-Si layer;
etching the poly-Si layer and the conductive material layer, and forming a first semiconductor layer, a first source electrode and a first drain electrode in the first region, and a second semiconductor layer, a second source electrode and a second drain electrode in the second region, wherein the first and second semiconductor layers are formed of the same material from the same processing;
forming a second gate insulating layer over the first and second source and drain electrodes;
forming a second gate electrode over the second region of the second gate insulating layer;
forming a protective layer on the second gate electrode;

etching the protective layer and the second gate insulating layer, and forming a via hole exposing one of the second source and drain electrodes; and

forming an OLED including a lower electrode electrically connected with the second source and drain electrodes through the via hole on the protective layer.

11. The method according to claim 10, further comprising crystallizing the a-Si layer into the poly-Si layer.

12. The method according to claim 10, further comprising: forming an amorphous silicon layer over the poly-Si layer; forming a conductive material layer over the a-Si layer; and etching the a-Si layer doped with impurities through an etching process for the poly-Si layer and the conductive material layer, and forming a first ohmic contact layer between the first semiconductor layer and the first source and first drain electrodes, and a second ohmic contact layer between the second semiconductor layer and the second source and second drain electrodes.

13. The method according to claim 10, further comprising forming a first etch stop layer over a first region of the poly-Si layer and a second etch stop layer over a second region of the poly-Si layer.

14. The method according to claim 13, further comprising forming the first and second etch stop layers along partial regions of the first and second semiconductor layers.

15. The method according to claim 10, further comprising: etching the second gate insulating layer and forming a first contact hole exposing one of the first source and drain electrodes; and

electrically connecting the second gate electrode with the first source and first drain electrodes through a second contact hole.

16. The method according to claim 10, further comprising: etching the second gate insulating layer and forming a second contact hole exposing one of the second source and second drain electrodes;

forming an interconnection electrically connected with the second source and second drain electrodes through the second contact hole along with the second gate electrode; and

electrically connecting the lower electrode with the interconnection by exposing the interconnection through the via hole.

17. The method according to claim 10, further comprising forming the first and second gate electrodes using the same material and the same process.

18. The method according to claim 10, wherein the OLED is formed by forming a pixel defining layer partially exposing the lower electrode over the protective layer, forming an organic layer including one or more emission layers over the lower electrode exposed by the pixel defining layer, and forming an upper electrode over the organic layer.

19. The method according to claim 10, further comprising: forming a planarization layer over the protective layer; forming a via hole by etching the protective layer and the planarization layer; and forming a lower electrode electrically connected with the second source and second drain electrodes through the via hole over the planarization layer.

* * * * *

专利名称(译)	有机发光二极管显示装置及其制造方法		
公开(公告)号	US20110108840A1	公开(公告)日	2011-05-12
申请号	US12/941930	申请日	2010-11-08
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
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摘要(译)

公开了一种有机发光二极管 (OLED) 显示装置及其制造方法。OLED显示装置包括多条扫描线，多条数据线和设置在扫描线与数据线交叉的区域中的多个像素，其中多个像素中的每个像素包括：开关晶体管，包括：第一栅电极，设置在第一栅电极上的第一半导体层，插入在第一栅电极和第一半导体层之间的第一栅极绝缘层，第一源电极和第一漏电极，包括第二半导体的驱动晶体管层，设置在第二半导体层上的第二栅电极，插入在第二栅电极和第二半导体层之间的第二栅极绝缘层，第二源电极和第二漏电极，以及与其电连接的有机发光二极管。驱动晶体管的第二源极和第二漏极，其中第一和第二半导体layers由相同的材料和相同的加工形成。

